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ABSTRACT OF THE DISCLOSURE

--A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.--

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ABSTRACT OF THE DISCLOSURE

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A microprocessor (50) includes a main central
5 processing unit (CPU) (70) and a separate direct memory
access (DMA) CPU (72) in a single integrated circuit
making up the microprocessor (50). The main CPU (70) has
a first 16 deep push down stack (74), which has a top item
register (76) and a next item register (78), respectively
10 connected to provide inputs to an arithmetic logic unit
(ALU) (80) by lines (82) and (84). An output of the ALU
(80) is connected to the top item register (76) by line
(86). The output of the top item register at (82) is also
connected by line (88) to an internal data bus (90). A
15 loop counter (92) is connected to a decrementer (94) by
lines (96) and (98). The loop counter (92) is
bidirectionally connected to the internal data bus (90) by
line (100). Stack pointer (102), return stack pointer
(104), mode register (106) and instruction register (108)
20 are also connected to the internal data bus (90) by lines
(110), (112), (114) and (116), respectively. The internal
data bus (90) is connected to memory controller (118) and
to gate (120). The gate (120) provides inputs on lines
(122), (124), and (126) to X register (128), program
25 counter (130) and Y register (132) of return push down
stack (134). The X register (128), program counter (130)
and Y register (132) provide outputs to internal address
bus (136) on lines (138), (140) and (142). The internal
address bus provides inputs to the memory controller (118)
30 and to an incrementer (144). The incrementer (144)
provides inputs to the X register, program counter and Y
register via lines (146), (122), (124) and (126). The DMA
CPU (72) provides inputs to the memory controller (118) on
line (148). The memory controller (118) is connected to a
35 RAM by address/data bus (150) and control lines (152).